Mechanical and Thermal Behavior of Copper Interconnects within Integrated Circuits

Alejandro Figueroa, Cody Kohler, Mariah Smith, Kaiyan Zhang
Faculty Advisor: Dr. Haiyan Wang
Industrial Sponsors: Dr. Karumbu Meyyappan and Dr. Aaron M. Scroggin

A study was done on the copper interconnects within the Intel Celeron G1840 Haswell and G1620 Ivy Bridge to determine if the copper metal lines displayed the same mechanical properties as copper thin films. Nano-indentation was performed on new samples and on samples that had been thermally treated to imitate 5 years of daily use. Hardness data trends from the new samples follow the trends expected from copper thin films by the hardness decreasing with increasing layer thickness. The thermally cycled samples show an overall decrease in hardness.

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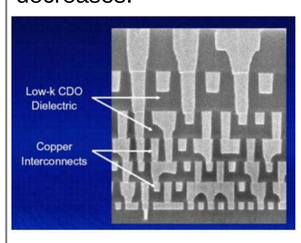
Problem Statement

- The first main goal of this project is to determine if the copper (Cu) interconnects within an integrated circuit display the same mechanical properties as Cu thin films.
- The second main goal of this project is to determine the effect of 5 years of CPU use on the mechanical properties of the Cu interconnects.

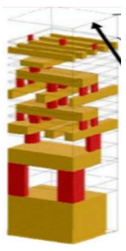
Project Background

CPU Geometry

Intel CPU's have complex geometry consisting of a Si die that is interlaced with Cu metal lines with varying sizes that are connected to each other known as Cu interconnects and the spaces in between are filled in with SiO2 dielectric. The metal lines are ordered in the Si die alternating between horizontal and vertical lines as the size decreases.



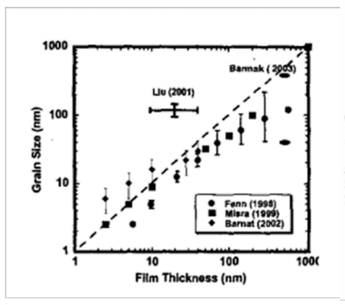
Side view of the Cu metal lines running through a Si die, decreasing in size.



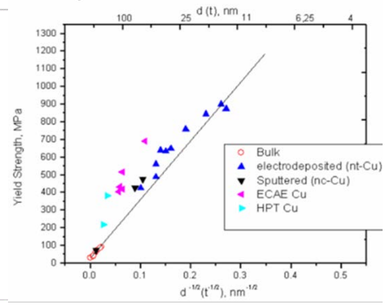
Three Dimensional view of Cu metal lines intersecting within the Si die.

Cu Thin Film Mechanical Properties

To discuss the material properties associated with Cu metal lines, it is necessary to address the material properties of Cu thin films. The first is the relationship between thin film thickness and grain size. As shown in the graph below, Cu grain size increases as a linear function with the film thickness. We can use this to identify the yield strength of the Cu interconnect without characterizing grain size. The graph below shows that the yield strength of a Cu thin film increases as a function of the square root of the grain size.



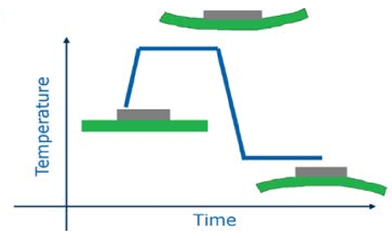
Graph of thin film thickness compared to grain size of Cu



Graph of yield strength compared to grain size of Cu thin films

Low Cycle Fatigue

A CPU experiences a wide temperature range of 20°C to 95°C throughout everyday use due to turning on and off a device. This temperature variation can cause thermo-mechanical fatigue stresses on the Si die, by the flexing of the substrate while the Si die remains stable. This is shown in the schematic below.



With long term operation, these stresses may lead to a failure after multiple temperature cycles. Temperature cycle testing is a method of acceleration testing for products that experience variation in temperature under a daily use basis. Since this experiment is focused on the effect of the extended thermal cycling on the Cu interconnects, a Coffin-Manson model was used to calculate the low cycle fatigue specifications to use in testing.

Hypothesis

Based on the Cu thin film behavior, we can expect there to be:

- A linear relationship between the grain size and the thickness of the Cu metal lines;
- The yield strength of the Cu metal lines to decrease with increasing thickness as it did with the thin films;
- The yield strength of the Cu interconnects to decrease after 5 years of usage.

Experimental Procedure

The samples that were examined were the Intel Celeron G1840 Haswell and the Intel Celeron G1620 Ivy Bridge.

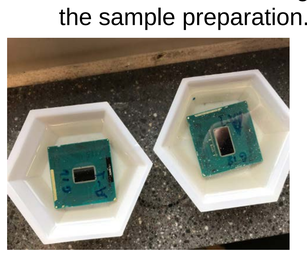
Sample Preparation

Integrated Heat Spreader Removal

Sample preparation began with removing the integrated heat spreader in order to properly view the Si die for sectioning. A schematic of this process is shown below.

Mounting

To analyze the microchips, the CPU samples would first be encased in epoxy to limit vibrational effects on the material that could be introduced during the sample preparation.

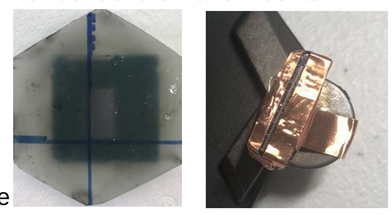


Sectioning

Samples were cut using a diamond saw along the length and width of the die approximately 1mm away from the die itself in both directions. This is done to expose interconnects oriented along both the width and the length due to the layered pattern of the interconnects. After SEM analysis, samples were cut to be 7mm thick to fit under the Nano-indenter.

Polishing

To fully expose the sample's surface a 800 grit sandpaper was used to grind away most of the remaining material near the sample surface. Once the surface had been exposed, a 15µm diamond lapping film was used for initial polishing of the sample. The sample was then prepared for SEM analysis with the use of a 6µm and then 1µm diamond lapping film.



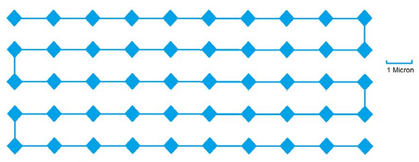
SEM Analysis

SEM analysis was used to determine the varying interconnect thicknesses and grain sizes with respect to the position. Samples that were thermally treated were also analyzed using a SEM to determine the failure modes induced by the flexing substrate. After Nano indentation, samples were examined with an SEM to view the indents.

Nano-indentation

Nano-indentation was conducted on each individual interconnect of varying size for the samples to be related to the thickness and grain size data that was obtained in SEM analysis. The Nano-indenter was programed to punch the sample every micron at a depth of 200nm, for 10 punches. Then it would move up one micron and punch 10 times and repeat this for 5 layers.

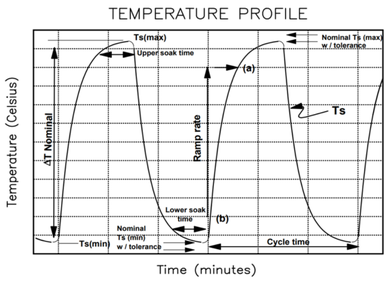
Picture of the Nano-indenter in use



Pattern of the indentation program

Thermal Cycle Testing

The Coffin-Mason Model was used with a temperature range of 0°C to 130°C. 614 cycles were calculated to put the CPU through 5 years of daily use. The samples were then put into a cycling furnace that heated the samples to 130°C and soaked for 10 minutes then cooled the samples to 0°C and soaked for another 10 minutes, for 614 cycles.



Schematic of the temperature cycling

Calculations for Accelerated Tests

$$Nf = C_o * (\Delta T - \Delta T_o)^{-q}$$

$$assume\ \Delta T_o \ll \Delta T$$

$$\frac{Nf_n = C_o * (\Delta T_n)^{-q}}{Nf_t = C_o * (\Delta T_t)^{-q}}$$

$$AF = \frac{Nf_n}{Nf_t} = \left(\frac{\Delta T_n}{\Delta T_t}\right)^{-q}$$

$$AF = \left(\frac{70\ C}{130\ C}\right)^{-4} = 12$$

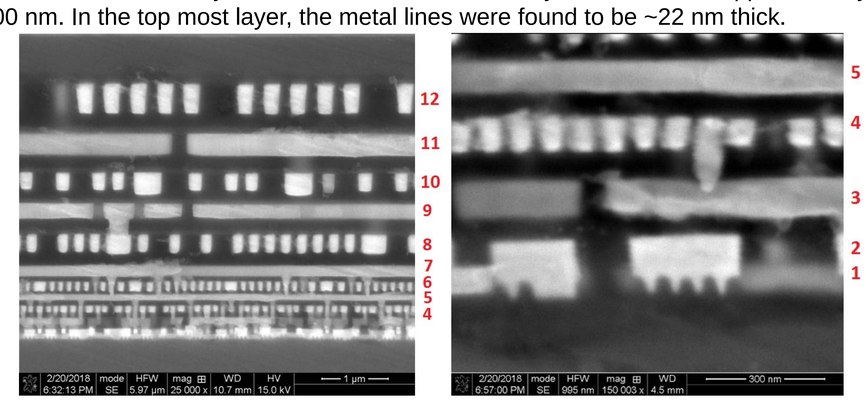
$$\frac{\#_n}{AF} = \#_t$$

$$\#_t = \frac{7300}{12} = 614$$

Results and Discussion

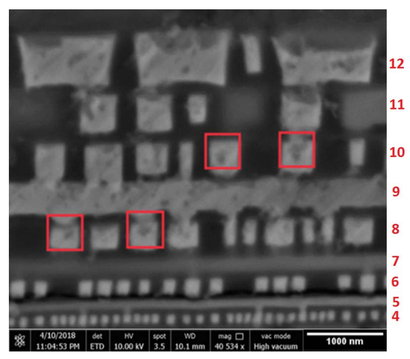
SEM Analysis

An SEM Image of the time zero G18 sample is shown below. It has 12 layers of copper thin film with different layer thicknesses. The thickest layer measured is approximately ~500 nm. In the top most layer, the metal lines were found to be ~22 nm thick.



A SEM image of the Cu interconnects before thermal cycling is shown on the left. An enlarged SEM image of the metal lines representing the thinnest layers is shown on the right.

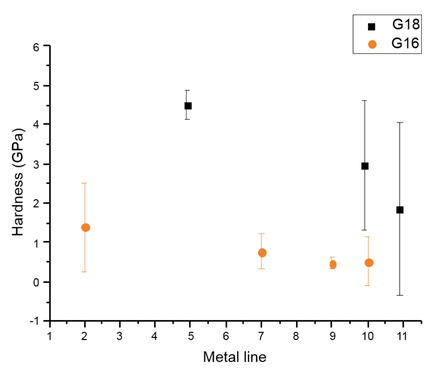
Surface roughness across the sample is approximately 1µm and the maximum Nano-indentation depth is 200 nm. Due to the limitation of the SEM system's resolution, as well as surface roughness, only a limited number of indents are identified through analysis. The red boxes surround the Cu lines where it is believed to have an indent. The plausible indents are 1µm apart which matches the Nano-indent program used.



Cu interconnects after Thermal Cycling

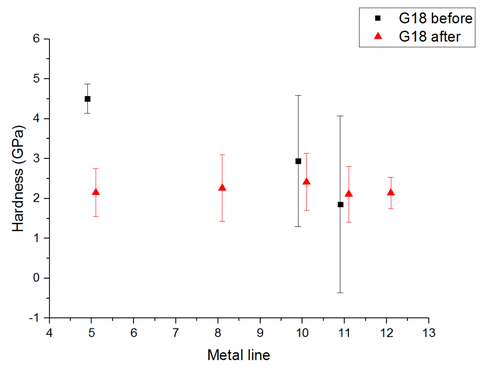
Properties Analysis of Cu Metal Lines

The Nano-indentation data indicates an increasing hardness trend as layer thickness decreases for both pre-cycled and post-cycled samples. This conforms to the hypothesis in which a decrease in grain size shows to increase the yield strength based on the Hall-Petch relation. There is a decrease in hardness as a result of thermal cycling on the sample. The hardness variation seems to increase as a result of thickness.



The graph to the left shows the hardness data for the Cu interconnects for G16 and G18 CPU samples. Depth refers to the contact depth from the starting point. The metal line number correlates to the labeled metal lines in the SEM images above.

The graph on the right shows the hardness data for the Cu interconnects for the G18 CPU before and after thermal cycling. Depth refers to the contact depth from the starting point. The metal line number correlates to the labelled metal lines in the SEM images above.



Summary

A trend between the layer thickness and hardness was found to be similar to the Cu thin films. Thermal cycling showed a decrease in hardness with a decrease in layer thickness. This data was conducted with small sample size to show the feasibility of this analysis and future work should be done to verify the confidence of the results.

Acknowledgements

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